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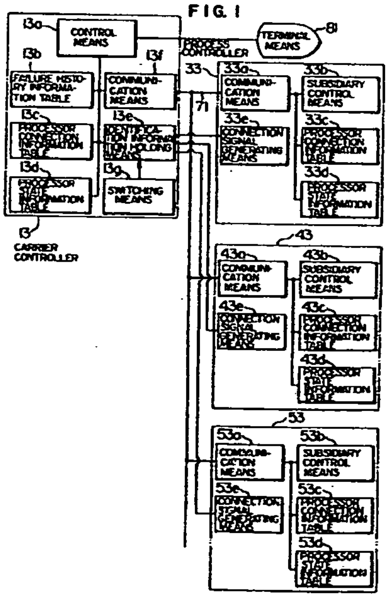
(54) Multiprocessing apparatus.

(57) Disclosed is a multiprocessing apparatus having a plurality of process processors (30, 40, 50) connected to a carrier processor (10) and controlled by a control system (13, 33, 43, 53), wherein there are provided connection information signal generating means (33e, 43e, 53e) for generating a connection information signal expressing information of connection of the plurality of process processors to the carrier processor, switching means (13g) for generating a registration information signal expressing information of registration of connection of the plurality of process processors to the carrier processor; and control means (13a) for carrying out a control process while logically judging a matching state between the connected process processors and the registered process processors by reference to the connection information and the registration information. Thus, it is possible to provide a multiprocessing apparatus in which process processors to be connected to the carrier processor can be increased or decreased in number easily and securely.

FIG. I


13a
CONTROL MEANS
PROCESS CONTROLLER
TERMINAL MEANS
81
13b
FAILURE HISTORY INFORMATION TABLE
13f
COMMUNICATION MEANS
13c
PROCESSOR CONNECTION INFORMATION TABLE
13e
IDENTIFICATION INFORMATION HOLDING MEANS
13d
PROCESSOR STATE INFORMATION TABLE
13g
SWITCHING MEANS
13
CARRIER CONTROLLER
71
33
33a
COMMUNICATION MEANS
33b
SUBSIDIARY CONTROL MEANS
33e
CONNECTION SIGNAL GENERATING MEANS
33c
PROCESSOR CONNECTION INFORMATION TABLE
33d
PROCESSOR STATE INFORMATION TABLE
43
43a
COMMUNICATION MEANS
43b
SUBSIDIARY CONTROL MEANS
43e
CONNECTION SIGNAL GENERATING MEANS
43c
PROCESSOR CONNECTION INFORMATION TABLE
43d
PROCESSOR STATE INFORMATION TABLE
53
53a
COMMUNICATION MEANS
53b
SUBSIDIARY CONTROL MEANS
53e
CONNECTION SIGNAL GENERATING MEANS
53c
PROCESSOR CONNECTION INFORMATION TABLE
53d
PROCESSOR STATE INFORMATION TABLE

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The present invention relates to a multiprocessing apparatus and particularly to a control system for generally controlling a plurality of processors connected to a carrier processor.

A semiconductor producing apparatus for flexibly executing a semiconductor wafer process by using a vacuum processing apparatus having a plurality of processors connected to a carrier processor has been disclosed in JP-A-63-129641.

In the case where the operation of the vacuum processing apparatus is continued while processors unnecessary for the wafer process and unworkable processors are connected to the carrier processor, a wafer process control sequence in which these processors are excluded can be set in this type semiconductor producing apparatus.

In such a vacuum processing apparatus, on the other hand, facilitation of alteration of the wafer process in the same apparatus configuration and increase or decrease of the number of the processors to cope with a variety of wafer processes is required.

The conventional vacuum processing apparatus is however insufficient in consideration of matching between the carrier processor and processors connected thereto. There arises a problem therefore in that if there is any mismatching between the two, the vacuum processing apparatus as a whole falls into the impossible of operation and the time required for clearing up the cause of the failure is so long that the working ratio of the apparatus becomes low. That is, in the vacuum processing apparatus in which controllers for the carrier processor and process processors connected thereto perform controlling operations relationally, if the relational operations are mistaken with respect to increase or decrease of the number of the processors or in connection with maintenance, both a wafer carrying operation and a process set by an operator cannot be performed so that the operation of the apparatus is stopped.

Furthermore, wasteful electric power is consumed in the conventional vacuum processing apparatus because main circuit electric sources are turned on even for processors not used. Moreover, because such main circuit electric sources are turned on, maintenance of processors not used cannot be made when the vacuum processing apparatus is in operation, so that the working ratio of the apparatus cannot be improved.

Therefore, an object of the present invention is to provide a multiprocessing apparatus in which processors to be connected to the carrier processor can be increased or decreased in number easily and securely.

In addressing the object, the present invention provides a multiprocessing apparatus comprising a carrier processor, a plurality of process processors connected to the carrier processor, and a control system for controlling the carrier processor and the plurality of process processors, wherein the apparatus further comprising: connection information signal generating means for generating a connection information signal expressing information of connection of the plurality of process processors to the carrier processor; switching means for generating a registration information signal expressing information of registration of connection of the plurality of process processors to the carrier processor; and control means for carrying out a control process while logically judging a matching state between the connected process processors and the registered process processors by reference to the connection information and the registration information.

Because the control means executes controlling while logically judging the matching state between the actually connected processors and the registered processors by reference to the processor connection information and the processor registration information, the trouble that process controlling is started while the processors are mismatched can be eliminated.

In the drawings:

Fig. 1 is a block diagram of a control system of a semiconductor vacuum processing apparatus as an embodiment of the present invention;

Fig. 2 is a constituent diagram showing the schematic configuration of the semiconductor vacuum processing apparatus;

Fig. 3 is a view showing the configuration of a processor connection information table in this embodiment;

Fig. 4 is a view showing the configuration of a processor information table in this embodiment;

Fig. 5 is a view showing the configuration of a processor connection state logical judgment table in this embodiment;

Fig. 6 is a flow chart of control executed by the main control means in this embodiment;

Fig. 7 is a flow chart of a control routine executed by the main control means in this embodiment;

Fig. 8 is a flow chart of a control routine executed by the main control means in this embodiment; and

Fig. 9 is a flow chart of a control routine executed by the main control means in this embodiment.

An embodiment of the present invention will be described hereunder in detail with reference to the drawings.

Fig. 1 is a block diagram showing a control system of a semiconductor vacuum processing apparatus as an embodiment of the present invention. The schematic structure of the semiconductor vacuum processing apparatus will be described with reference to Fig. 2 before description of the operation of the control system.

Referring to Fig. 2, there is shown a semiconductor vacuum processing apparatus having three processors connected to a carrier processor. The carrier processor 10 has one side to which a load lock chamber 21 and an unload lock chamber 22 are connected, and the other three sides to which process processors 30, 40 and 50 for processing semiconductor wafers are respectively connected. Process processing chambers 31, 41 and 51 of the process processors 30, 40 and 50 are connected to a carrier processing chamber 11 of the carrier processor 10 respectively through gate valves 61, 62 and 63 so that semiconductor wafers can be carried by an arm 12-1, 12-2, 12-3 of the carrier processing chamber 11 through the gate valves 61, 62 and 63 opened. The wafers are transported between arms through stages 14-1 and 14-2. Electrodes 32, 42 and 52 for mounting semiconductor wafers thereon and discharge devices (not shown) for processing the semiconductor wafers are provided in the process processing chambers 31, 41 and 51, respectively. Further, vacuum exhaust devices for exhausting the process processing chambers are connected to the process processing chambers 31, 41 and 51, respectively.

A control system for controlling those parts has a carrier controller 13 for controlling the carrier processor 10, a process controller 33 for controlling the process processor 30, a process controller 43 for controlling the process processor 40, and a process controller 53 for controlling the process processor 50.

This semiconductor vacuum processing apparatus is systematized so that a semiconductor wafer to be processed is picked up from a load cassette (not shown) to the load lock chamber 21 by an air carrier (not shown) and then carried into arbitrary one of the process processing chambers 31, 41 and 51 by the arm 12-1, 12-2, 12-3, and the processed semiconductor wafer is carried out to the unload lock chamber 22 and then returned to the original cassette or another cassette by the air carrier.

Examples of processes executed by the process processors 30, 40 and 50 are a film forming process, a CVD process, an etching process, etc. The process processors 30, 40 and 50 execute these processes under control by the process controllers 33, 43 and 53, respectively.

Fig. 1 shows in detail the configuration of the control system.

The carrier controller 13 has a main control means 13a, a failure history information table 13b, a processor connection information table 13c, a processor state information table 13d, an identification information holding means 13e, and a communication means 13f which are connected to the main control means 13a. Further, the carrier controller 13 has a switching means 13g connected to the identification information holding means 13e.

The carrier controller 13 controls the arm 12-1, 12-2, 12-3 and the gate valves 61, 62 and 63 so that a semiconductor wafer to be processed is carried from the load lock chamber 21 into arbitrary one of the process processors 30, 40 and 50 and that the processed semiconductor wafer is carried out from arbitrary one of the process processors 30, 40 and 50 to the unload lock chamber 22, and at the same time, controls the process controllers 33, 43 and 53 so that predetermined processes are respectively executed by the process processors 30, 40 and 50.

The failure history information table 13b is a table for storing information of failures (for example, discharge failure, pressure failure, electric source failure, etc.) occurring in the process processors 30, 40 and 50.

As shown in Fig. 3, the processor connection information table 13c is a table for storing the relations in connection between the carrier processor 10 and the process processors 30, 40 and 50.

As shown in Fig. 4, the processor state information table 13d is a table for storing information for identification of the states (the states of control by the carrier controller 13 and the process controllers 33, 43 and 53) of the process processors 10, 30, 40 and 50.

The identification information holding means 13e stores a registration information signal given from the switching means 13g and a connection information signal given from a connection signal generating means which will be described later, and holds these signals as information for identification as to whether the process processors 30, 40 and 50 are validly connected to the carrier processor 10, on the basis of a logical judgment as shown in Fig. 5.

The communication means 13f has a bidirectional communication function. A CSMA/CD communication system or a token-ring communication system is used as the communication means 13f. The communication means 13f communicates with the process controllers 33, 43 and 53 through a communication medium 71 such as a stranded cable, a coaxial cable, etc.

The switching means 13g generates a registration information signal for registration as to whether predetermined one or ones of the process processors 30, 40 and 50 to be connected to the carrier processor 10 are connected to signal lines respectively assigned thereto. A dip switch operated by an operator, or the like, is used as the switching means 13g.

Alternatively, it is considered that the registration information may be stored in the switching means 13g. For example, an electrically erasable memory (EEPROM) may be used as the switching means 13g to store the registration information preliminarily.

The process controllers 33, 43 and 53 are provided independently of the carrier controller 13 and connected so that signal transfer is made through the communication medium 71. The process controllers 33, 43 and 53 respectively have communication means 33a, 43a and 53a, subsidiary control means 33b, 43b and 53b, processor connection information tables 33c, 43c and 53c, and processor state information tables 33d, 43d and 53d which are connected to the communication means 13f through the communication medium 71. Further, the process controllers 33, 43 and 53 respectively have connection signal generating means 33e, 43e and 53e connected to the identification information holding means 13e.

The communication means 33a, 43a and 53a, processor connection information tables 33c, 43c and 53c and processor state information tables 33d, 43d and 53d are respectively formed in the same manner as the communication means 13f, processor connection information table 13c and processor state information table 13d of the carrier controller 13.

The subsidiary control means 33b, 43b and 53b execute predetermined control processes individually in response to control signals received from the carrier controller 13 and then return control results and control states.

The connection signal generating means 33e, 43e and 53e are means for respectively generating connection information signals expressing the fact that the process processors 30, 40 and 50 are connected to the carrier processor 10. Signals (for example, breaker-on signals) expressing the fact that the process controllers 33, 43 and 53 are connected to electric source circuits, or other digital signals, are used in the connection signal generating means 33e, 43e and 53e.

As another method by which the carrier processor 10 recognizes the connection information, it is considered that (i) the carrier processor may receive the connection information from the respective process processors by the communication means and may recognize the connection information or that (ii) the carrier processor may make a request for the connection information to process processors connected to the carrier processor and may recognize the connection information.

A terminal means 81 is controlled by the main control means 13a and used for the double purpose of displaying guidance for operators and of inputting the sequence of processes to be executed by the process processors as relational information of process processor and process receipe number.

A control process executed by the main control means 13a in the operation of the semiconductor vacuum processing system will be described hereunder with reference to Figs. 6 through 9.

When a main electric source switch (not shown) for the semiconductor vacuum processing system is turned on in the step 110, the situation of the routine goes to the step 120 in which control electric sources for the process controllers 33, 43 and 53 are validated (turned on). Then, the situation of the routine goes to the step 130 in which information stored in the identification information holding means 13e is confirmed, and to the step 140 in which a judgment as to whether there is any processor invalid in connection is made for displaying the connection state and the guidance for restoration. When there is any processor invalid in connection, the situation of the routine goes to the step 150 shown in Fig. 7. When there is no processor invalid in connection, the situation of the routine goes to the step 220 shown in Fig. 8.

The step 150 is a step for branching the control correspondingly to the cause of invalidity in connection. In the step 150, information stored in the identification information holding means 13e is judged logically. When registration information and connection information corresponding to the processor invalid in connection respectively express "unregistered" and "connected", the situation of the routine goes to the step 160. When the registration information and the connection information respectively express "registered" and "unconnected", the situation of the routine goes to the step 170. When the registration information and the connection information respectively express "unregistered" and "unconnected", the situation of the routine goes to the step 220 shown in Fig. 8.

The state in which the registration information and the connection information respectively express "unregistered" and "connected" shows the case where the operation of registering a process processor by the switching means is idled after connection of the process processor. Accordingly, in the step 160, guidance for turning the switching means 13g to "registered" with respect to the process processor is displayed on the terminal means 81. Then, in the step 180, the inputting of the registration information signal given from the switching means 13g is confirmed. Thereafter, the situation of the routine goes to the step 220 shown in Fig. 8.

The state in which the registration information and the connection information respectively express "registered" and "unconnected" shows the case where the information signal of "connected" from the connection information generating means cannot be inputted because of disconnection of the process processor for maintenance or because of failure in the control electric source or the signal circuit. Accordingly, in the step 170, guidance for requesting an input for selection as to whether the process processor is regarded as "unconnected" (neglected) or whether the process processor is used after restoration to a valid state (restored) is displayed on the terminal means 81. Then, in the step 190, the inputting of selection given from the terminal means 81 is checked. When the selection is "neglected", guidance for operating the switching means to make the process processor "unregistered" is displayed on the terminal means 81 in the step 200. When the selection is "restored", guidance for restoring the process processor is displayed on the terminal means 81 in the step 210.

After the aforementioned control process is executed, in the step shown in Fig. 8, the process processor validly connected to the carrier processor is confirmed and registered by reference to the connection information and the registration information stored in the identification information holding means 13e. Then, in the step 230, a judgment is made by reference to the failure history information table 13d as to whether the "validly connected" process processor is normal or abnormal. Then, in the step 240, a judgment is made as to whether there is any abnormal process processor.

When there is no abnormal process processor, the situation of the routine goes to the step 250 in which the main circuit electric source for the normal process processor is turned on.

When there is any abnormal process processor, the situation of the routine goes to the step 260 in which the abnormal process processor and the abnormal state thereof are displayed on the terminal means 81. Furthermore, in the step 270, a judgment is made as to whether the semiconductor vacuum processing apparatus can be operated while the abnormal process processor is connected to the carrier processor. When the apparatus can be operated, guidance for operating the switching means 13g to make registration information corresponding to the abnormal process processor "unregistered" is displayed on the terminal means 81 in the step 280 and then the situation of the routine goes back to the step 250. When the system cannot be operated, guidance for restoring the abnormal process processor is displayed on the terminal means 81 in the step 290.

Then, in the step 300, a process processor connection state judging and setting routine is carried out and then the situation of the routine goes to the vacuum processing operation.

The routine of the step 300 is shown in Fig. 9. In the step 301, identification information stored in the identification information holding means 13e is read and subjected to a judgment as to whether the process processors 30, 40 and 50 are validly connected, so that judgment results are stored in the processor connection information table 13c. Because this embodiment shows the case where three process processors 30, 40 and 50 are validly connected to the carrier processor 10, the data stored in the processor connection information table 13c is "00001111" (validly connected: 1, unconnected or invalidly connected: 0).

Then, in the step 302, the connection information is transmitted to the process controller 33 and stored in the processor connection information table 33c of the processor controller 33.

Like this, in the step 303, the connection information is transmitted to the process controller 43 and stored in the processor connection information table 43c of the processor controller 43.

Also like this, in the step 304, the connection information is transmitted to the process controller 53 and stored in the processor connection information table 53c of the processor controller 53.

In the vacuum processing operation, a process of checking the states of the process processors 10, 30, 40 and 50 at any time and altering the data stored in the processor state information tables 13d, 33d, 43d and 53d on the basis of the state information is carried out. The process processors having the connection information and the state information stored therein can carry out respective processes while control signals are transferred, on the mutual recognition of information of the process processors.

As described above, according to the present invention, matching between an actually connected process processor and a registered process processor is judged logically by reference to processor connection information and processor registration in formation, so that the trouble that process controlling is started while the two are mismatched can be eliminated.

Furthermore, the mismatched process processor can be used or restored properly through displaying the mismatching state on the terminal means, so that the working ratio of the system can be improved.

Claims

1. A multiprocessing apparatus comprising a carrier processor (10), a plurality of process processors (30, 40, 50) connected to the carrier processor, and a control system (13, 33, 43, 53) for controlling said carrier processor and said plurality of process processors, wherein

said apparatus further comprising: connection information signal generating means (33e, 43e, 53e) for generating a connection information signal expressing information of connection of said plurality of process processors to said carrier processor; switching means (13g) for generating a registration information signal expressing information of registration of connection of said plurality of process processors to said carrier processor; and control means (13a) for carrying out a control process while logically judging a matching state between the connected process processors and the registered process processors by reference to the connection information and the registration information.

2. A multiprocessing apparatus according to Claim 1, wherein said multiprocessing apparatus further comprises a terminal means (81), and said control means controls said terminal means to display guidance based on the matching state.

3. A multiprocessing apparatus according to Claim 1, wherein said multiprocessing apparatus further comprises a failure history storage means (13b) for storing information of the history of failures occurring in said multiprocessing apparatus, and said control means executes a process of controlling the connected process processors by reference to the failure history information.

4. A multiprocessing apparatus according to Claim 2, wherein said multiprocessing apparatus further comprises a failure history storage means (13b) for storing information of the history of failures occurring in said multiprocessing apparatus, and said control means executes a process of controlling the connected process processors by reference to the failure history information.

5. A multiprocessing apparatus according to Claim 1, wherein said multiprocessing apparatus further comprises a processor state information storage means (13c) for storing information of the states of the respective process processors, and said control means executes a process of controlling the connected process processors by reference to the processor state information.

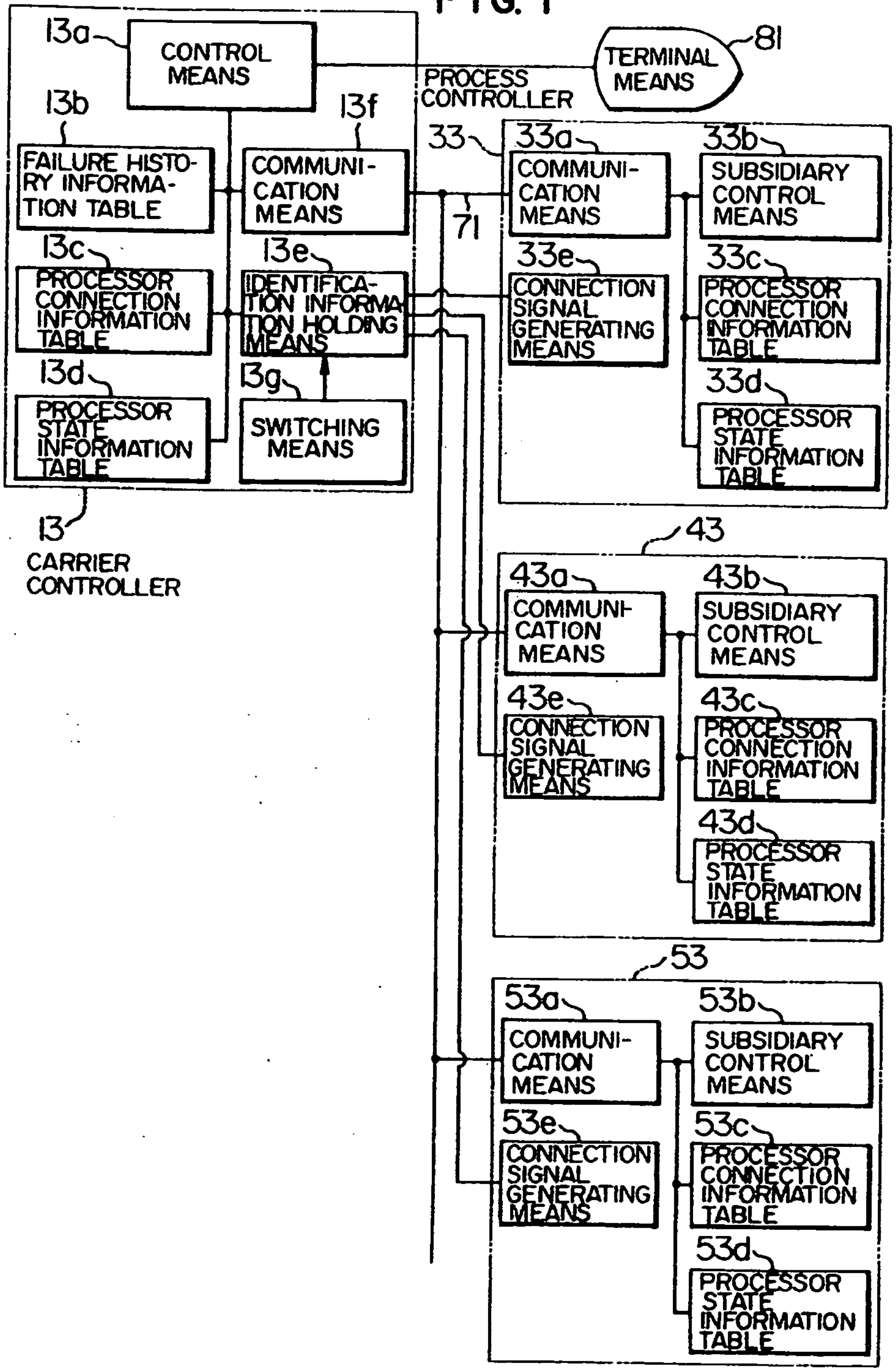
6. A multiprocessing apparatus according to Claim 2, wherein said multiprocessing apparatus further comprises a processor state information storage means (13c) for storing information of the states of the respective process processors, and said control means executes a process of controlling the connected process processors by reference to the processor state information.

7. A multiprocessing apparatus according to Claim 3, wherein said multiprocessing apparatus further comprises a processor state information storage means (13c) for storing information of the states of the respective process processors, and said control means executes a process of controlling the connected process processors by reference to the processor state information.

8. A multiprocessing apparatus comprising a carrier processor (10), a plurality of process processors (30, 40, 50) connected to said carrier processor, a plurality of process controllers (33, 43, 53) for respectively controlling said plurality of process processors, and a carrier controller (13) for controlling said carrier processor and said plurality of process controllers, wherein each of said process controllers includes connection information signal generating means (33e, 43e, 53e) for generating a connection information signal expressing information of connection of said process processor to said carrier processor, and said carrier controller includes switching means (13g) for generating a registration information signal expressing registration of connection of said process processor to said carrier processor, and control means (13a) for carrying out a control process while logically judging a matching state between the connected process processors and the registered process processors by reference to the connection information and the registration information.

9. A multiprocessing apparatus according to Claim 8, wherein said process controllers and said carrier controller respectively includes processor connection information storage means (13c, 33c, 43c, 53c), and said control means controls said processor connection information storage means to store information expressing the relations in connection between said process processors.

FIG. 1


13a
CONTROL MEANS
PROCESS CONTROLLER
TERMINAL MEANS
81
13b
FAILURE HISTORY INFORMATION TABLE
13f
COMMUNICATION MEANS
33
71
33a
COMMUNICATION MEANS
33b
SUBSIDIARY CONTROL MEANS
13c
PROCESSOR CONNECTION INFORMATION TABLE
13e
IDENTIFICATION INFORMATION HOLDING MEANS
33e
CONNECTION SIGNAL GENERATING MEANS
33c
PROCESSOR CONNECTION INFORMATION TABLE
13d
PROCESSOR STATE INFORMATION TABLE
13g
SWITCHING MEANS
33d
PROCESSOR STATE INFORMATION TABLE
13
CARRIER CONTROLLER
43
43a
COMMUNICATION MEANS
43b
SUBSIDIARY CONTROL MEANS
43e
CONNECTION SIGNAL GENERATING MEANS
43c
PROCESSOR CONNECTION INFORMATION TABLE
43d
PROCESSOR STATE INFORMATION TABLE
53
53a
COMMUNICATION MEANS
53b
SUBSIDIARY CONTROL MEANS
53e
CONNECTION SIGNAL GENERATING MEANS
53c
PROCESSOR CONNECTION INFORMATION TABLE
53d
PROCESSOR STATE INFORMATION TABLE

F I G. 2

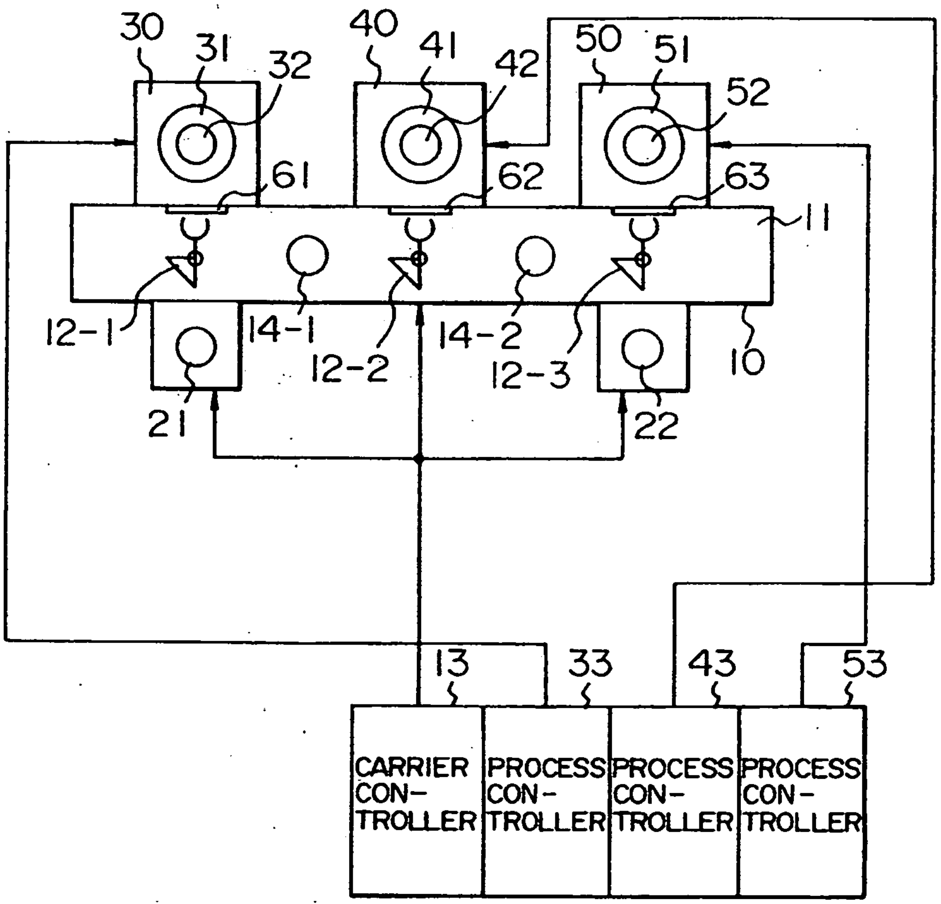

12-1
14-1
12-2
14-2
12-3
CARRIER CON-TROLLER
PROCESS CON-TROLLER
PROCESS CON-TROLLER
PROCESS CON-TROLLER

FIG. 3

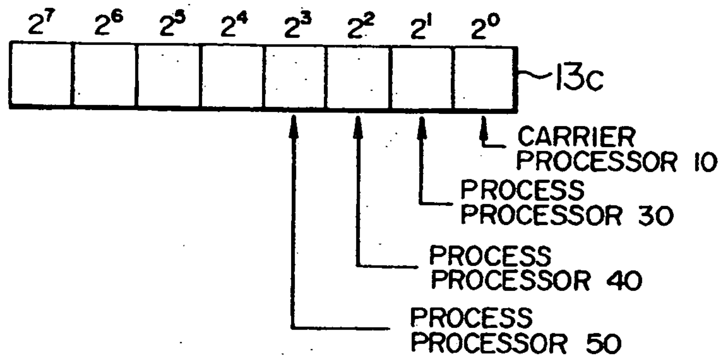


FIG. 5

NO. \ INFORMATION	PROCESSOR CONNECTION INFORMATION	REGISTRATION INFORMATION	RECOGNITION
PROCESSOR (1)	CONNECTED	REGISTERED	VALID
PROCESSOR (2)	UNCONNECTED	REGISTERED	INVALID
PROCESSOR (3)	CONNECTED	UNREGISTERED	INVALID
PROCESSOR (4)	UNCONNECTED	UNREGISTERED	INVALID

F I G. 4

2^7							2^0	
				AUTOMATIC RUNNING	ABNOR-MAL	EXECU-TION	STANDING-BY	CARRIER PROCESSOR 10
				AUTOMATIC RUNNING	ABNOR-MAL	EXECU-TION	STANDING-BY	PROCESS PROCESSOR 30
				AUTOMATIC RUNNING	ABNOR-MAL	EXECU-TION	STANDING-BY	PROCESS PROCESSOR 40
				AUTOMATIC RUNNING	ABNOR-MAL	EXECU-TION	STANDING-BY	PROCESS PROCESSOR 50

13d

FIG. 6

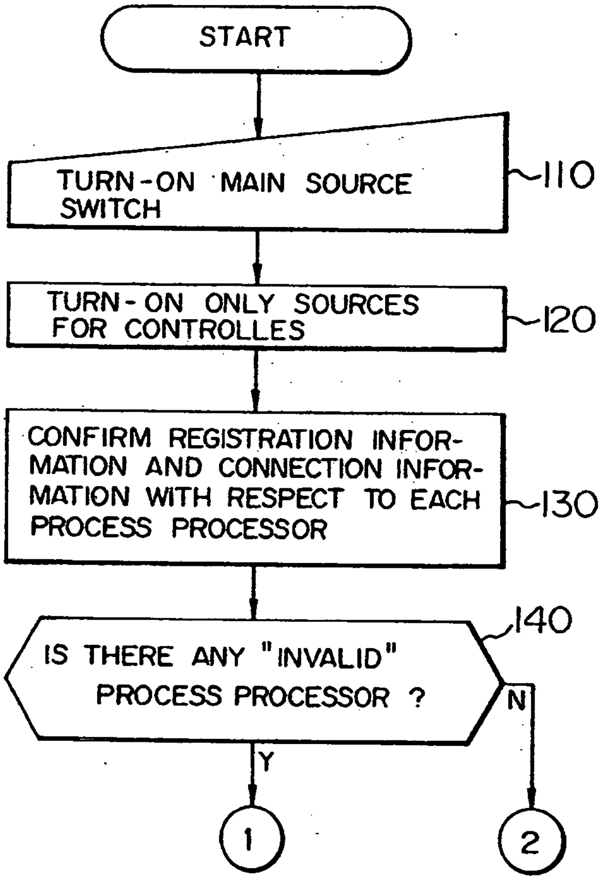

START
TURN-ON MAIN SOURCE SWITCH
110
TURN-ON ONLY SOURCES FOR CONTROLLES
120
CONFIRM REGISTRATION INFORMATION AND CONNECTION INFORMATION WITH RESPECT TO EACH PROCESS PROCESSOR
130
IS THERE ANY "INVALID" PROCESS PROCESSOR ?
140
N
Y
1
2

FIG. 7

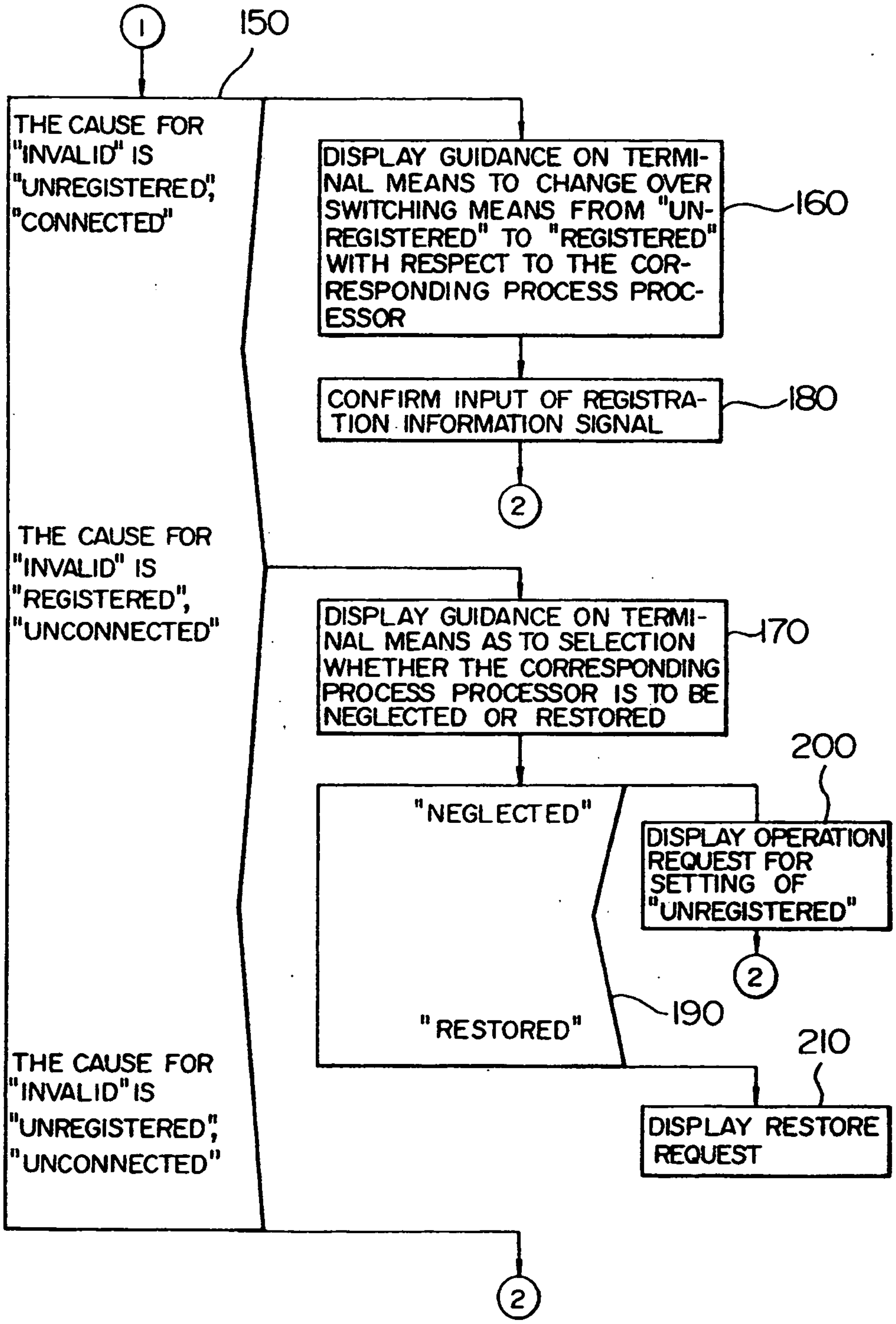

1
150
THE CAUSE FOR "INVALID" IS "UNREGISTERED", "CONNECTED"
DISPLAY GUIDANCE ON TERMINAL MEANS TO CHANGE OVER SWITCHING MEANS FROM "UNREGISTERED" TO "REGISTERED" WITH RESPECT TO THE CORRESPONDING PROCESS PROCESSOR
160
CONFIRM INPUT OF REGISTRATION INFORMATION SIGNAL
180
2
THE CAUSE FOR "INVALID" IS "REGISTERED", "UNCONNECTED"
DISPLAY GUIDANCE ON TERMINAL MEANS AS TO SELECTION WHETHER THE CORRESPONDING PROCESS PROCESSOR IS TO BE NEGLECTED OR RESTORED
170
200
"NEGLECTED"
DISPLAY OPERATION REQUEST FOR SETTING OF "UNREGISTERED"
2
"RESTORED"
190
210
DISPLAY RESTORE REQUEST
THE CAUSE FOR "INVALID" IS "UNREGISTERED", "UNCONNECTED"
2

FIG. 8

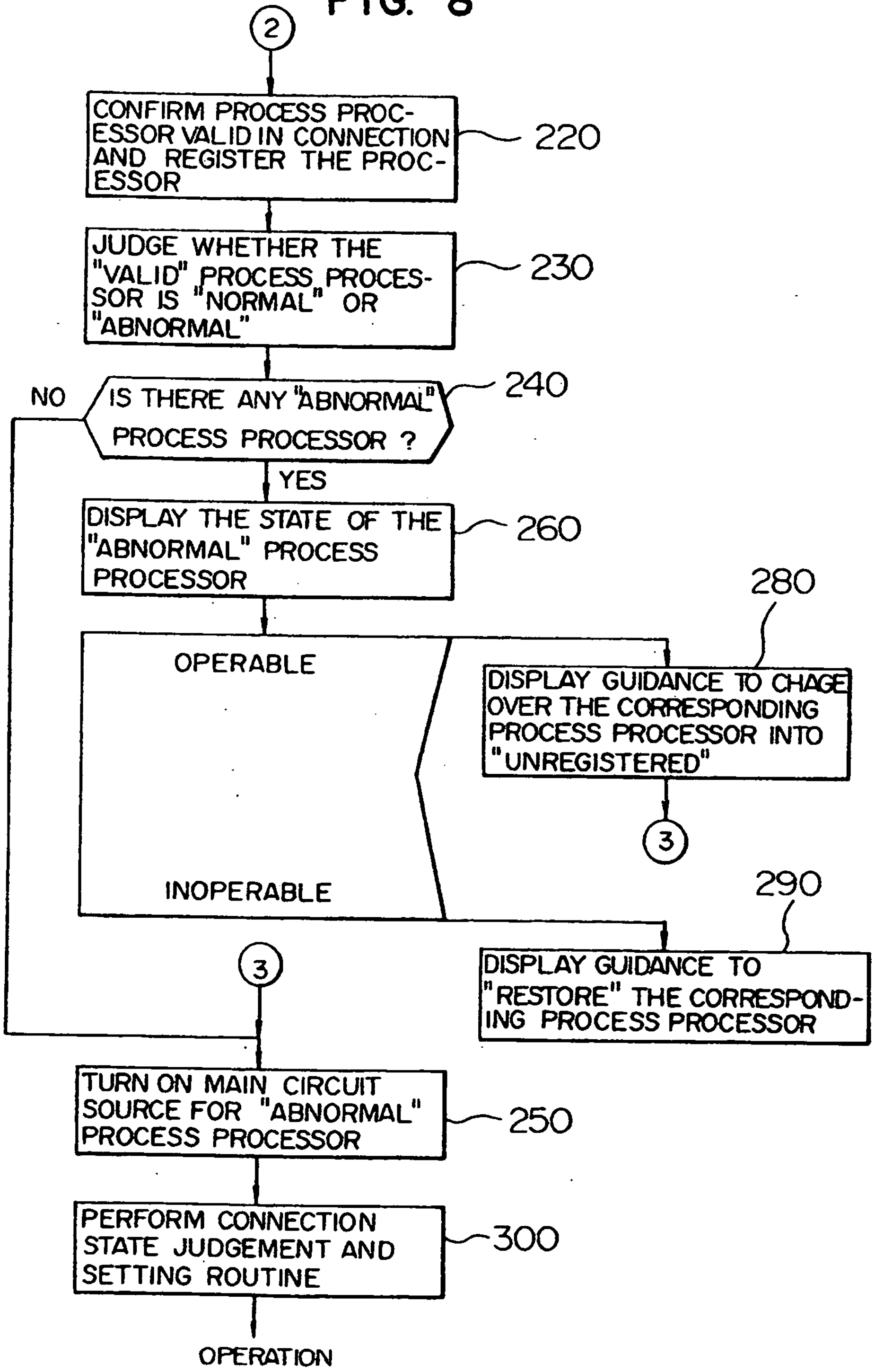
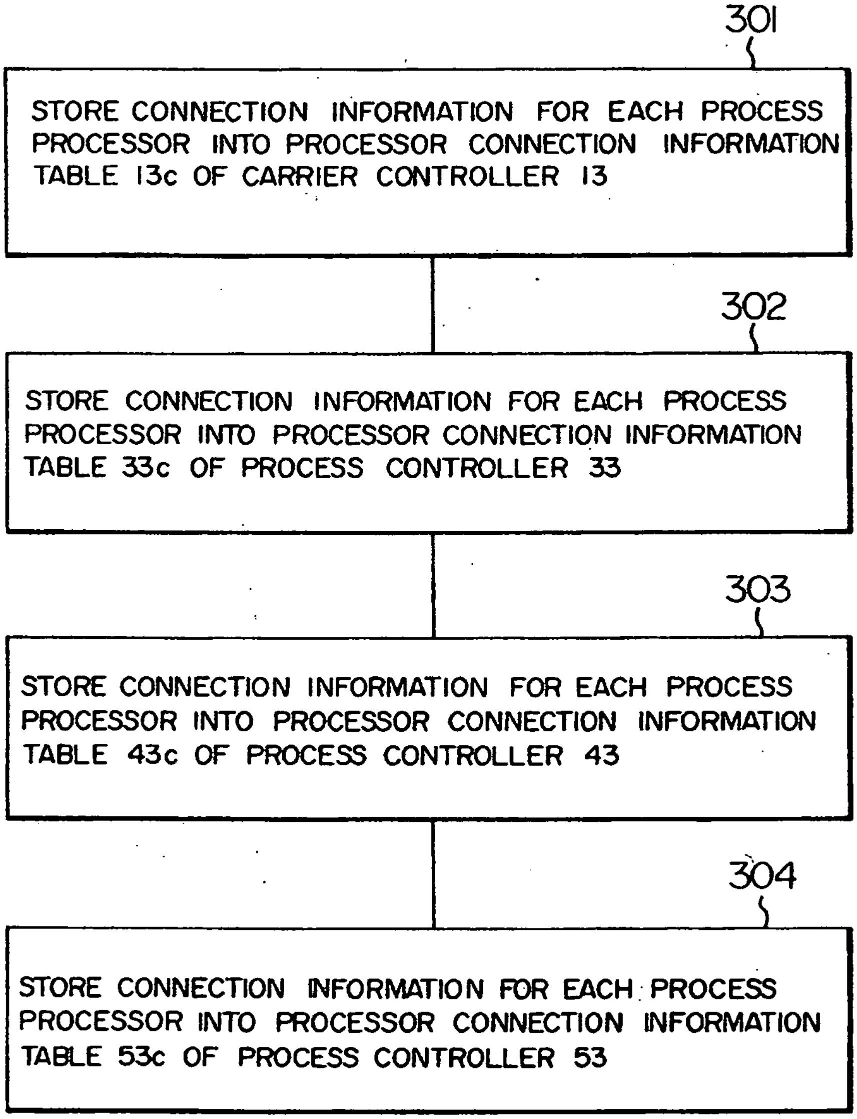

2
CONFIRM PROCESS PROCESSOR VALID IN CONNECTION AND REGISTER THE PROCESSOR
220
JUDGE WHETHER THE "VALID" PROCESS PROCESSOR IS "NORMAL" OR "ABNORMAL"
230
NO
IS THERE ANY "ABNORMAL" PROCESS PROCESSOR ?
240
YES
DISPLAY THE STATE OF THE "ABNORMAL" PROCESS PROCESSOR
260
280
OPERABLE
DISPLAY GUIDANCE TO CHAGE OVER THE CORRESPONDING PROCESS PROCESSOR INTO "UNREGISTERED"
3
INOPERABLE
290
3
DISPLAY GUIDANCE TO "RESTORE" THE CORRESPONDING PROCESS PROCESSOR
TURN ON MAIN CIRCUIT SOURCE FOR "ABNORMAL" PROCESS PROCESSOR
250
PERFORM CONNECTION STATE JUDGEMENT AND SETTING ROUTINE
300
OPERATION

FIG. 9


301
STORE CONNECTION INFORMATION FOR EACH PROCESS PROCESSOR INTO PROCESSOR CONNECTION INFORMATION TABLE 13c OF CARRIER CONTROLLER 13
302
STORE CONNECTION INFORMATION FOR EACH PROCESS PROCESSOR INTO PROCESSOR CONNECTION INFORMATION TABLE 33c OF PROCESS CONTROLLER 33
303
STORE CONNECTION INFORMATION FOR EACH PROCESS PROCESSOR INTO PROCESSOR CONNECTION INFORMATION TABLE 43c OF PROCESS CONTROLLER 43
304
STORE CONNECTION INFORMATION FOR EACH PROCESS PROCESSOR INTO PROCESSOR CONNECTION INFORMATION TABLE 53c OF PROCESS CONTROLLER 53

European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 92 30 7052

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 377 331 (PITNEY BOWES INC) 11 July 1990 * column 12, line 3 - column 14, line 21 * * column 16, line 58 - column 17, line 44 * * figure 5 * ---	1-9	G05B19/04
A	US-A-4 564 913 (TOSHIHIKO YOMOGIDA) 14 January 1986 * column 3, line 21 - column 7, line 35 * * figure 1 * ---	1,2,8	
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TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G05B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 OCTOBER 1992	NETTESHEIM J.

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